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| 10/035,660 | 12/28/2001 | Choon-Seng Tan | P01-3978 | 4624 |

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| EXAMINER | |
|---|---|
| PATEL, NIKETA I | |

| ART UNIT | PAPER NUMBER |
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| 2182 | 5 |

DATE MAILED: 03/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 10/035,660 | Applicant(s) TAN ET AL. | |
|---|---|---|---|
| | Examiner Niketa I. Patel | Art Unit 2182 | |

*-- The MAILING DATE of this communication appears on the cover sheet with th correspondenc address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jantz U.S. Patent Number: 5,944,838 (hereinafter referred to as "*Jantz*".)

3. **Referring to claim 1**, *Jantz* teaches a method of controlling a failover process in a data storage system including a host, a host bus adapter, a communication fabric including data paths, and standby and active storage controllers, comprising: detecting with the host bus adapter [see column 1 – lines 25-48, 'RDAC'; column 5 – lines 28-41] a failover condition [see column 2 – lines 19-33]; responsive to the detecting, operating the host bus adapter to match the failover condition to a particular failover action in a failover rule set [see column 8 – lines 45-67; column 9 – 10-67]; and performing with the host bus adapter the matched failover action [see column 8 – lines 45-67; column 9 – 10-67, 'RDAC'] although, *Jantz* does not explicitly set forth the limitation of detecting failover condition with a host bus adapter. *Jantz* teaches to perform detecting failover condition with a software module called "RDAC" that may be operable within a host bus adapter [see column 1 – lines 25-48] to enable it to encompass control of a larger number of I/O path elements in its failure recovery techniques.

One of ordinary skill in the art would have clearly recognized that it was quite advantageous for the host bus adapter of the *Jantz* to detect failover condition and responding to

the failover condition to encompass control of a large number of I/O path elements in its failure recovery techniques. It is for this reason that one of ordinary skill in the art would have been motivated to implement failover detecting module onto the host bus adapter in order to encompass control of a large number of I/O path elements in its failure recovery techniques.

4. **Referring to claim 2**, the method of *Jantz* as modified above in claim 1, teaches that the detecting, operating, and the failover action performing are completed without acts initiated by the host [see column 1 – lines 25-48, 'RDAC'.]

5. **Referring to claim 3**, the method of *Jantz* as modified above in claim 1, *Jantz* teaches that the detecting includes identifying a particular failure type and wherein the particular fail over action is selected from an action subset corresponding to the particular failure type [see column 1 – lines 25-48, 'RDAC'; column 2 – lines 19-33.]

6. **Referring to claim 4**, the method of *Jantz* as modified above in claim 1, *Jantz* teaches that the failure type is selected from the group consisting of inter-controller link down, the active storage controller failed, the standby controller failed, an active path failed, and a standby path failed [see column 2 – lines 19-33.]

7. **Referring to claim 5**, although the method of *Jantz* as modified above in claim 1, teaches to detecting with the host bus adapter a failover condition, *Jantz* is silent about prior to the performing, determining with the host bus adapter if all active paths have failed and if all active paths determined failed, skipping the failover action performing when the host bus adapter determines either all other available paths have failed or a standby path is marked as unusable. However, this feature is deemed to be inherent to the *Jantz* system as lines 19-33 of column 2, lines 45-67 of column 8 and lines 10-67 of column 9 teaches to determine a failover condition

and in response to the failover condition rerouting data through an alternate rout. If all the routs have failed then the system would not be able reroute the data, therefore it would have to skip the performance of the failover action.

8. **Referring to claim 6**, the method of *Jantz* as modified above in claim 1 teaches, further including after the failover action performing, operating the host bus adapter to initiate failback when a controller in a preferred slot is replaced, when the controller in the preferred slot is rebooted, and when unusable paths become usable [see column 7 – lines 5-24.]

9. **Referring to claim 7**, the method of *Jantz* as modified above in claim 1 teaches to use multiple paths to transmit/receive data between the host and the storage devices [see column 5 – lines 28-41] however, *Jantz* is silent on performing load distribution with the host bus adapter between the host and the controllers.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention that it was old and well known in the computer art to get the advantage of saving valuable resources by using multiple paths to balance load of incoming and outgoing data by distributing it over multiple paths. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to perform load distribution with the host bus adapter to get this advantage.

10. **Referring to claims 8 and 19**, *Jantz* is silent about enforcing with the host bus adapter anti-thrashing rules comprising preventing the performing from being completed more than set number of times per pre-set monitoring interval.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention that an anti-thrashing was an old and well-known type of safeguard. It would have

been obvious to one of ordinary skill in the art at the time of applicant's invention to implement anti-thrashing safeguard to prevent the system from falling into an endless loop.

11. **Referring to claim 9**, *Jantz* teaches a host bus adapter for managing failover and failback processes [see column 1 – lines 25-48, 'RDAC'; column 7 – lines 5-24] within a data storage system having a host server, a communication fabric [see figure 1 – elements 104, 105, 106; column 5 – lines 8-41], at least one active storage controller [see figure 1 – element 110], and at least one standby storage controller [see figure 1 – element 112 ], comprising: a connector linking the host bus adapter to a processor of the host server [see figure 3 – element 304] ; a port linking the host bus adapter to the communication fabric configured for transmitting and receiving digital information [see figure 3 – elements 302, 304, 312]; and a failover mechanism detecting a redundancy failure in the data storage system and in response, initiating failover actions [see column 1 – lines 25-48, 'RDAC'; column 8 – lines 45-67; column 9 – 10-67, 'RDAC'] although, *Jantz* does not explicitly set forth the limitation of detecting failover condition with a host bus adapter. *Jantz* teaches to perform detecting failover condition with a software module called "RDAC" that may be operable within a host bus adapter [see column 1 – lines 25-48] to enable it to encompass control of a larger number of I/O path elements in its failure recovery techniques.

One of ordinary skill in the art would have clearly recognized that it was quite advantageous for the host bus adapter of the *Jantz* to detect failover condition and responding to the failover condition to encompass control of a large number of I/O path elements in its failure recovery techniques. It is for this reason that one of ordinary skill in the art would have been

motivated to implement failover detecting module onto the host bus adapter in order to encompass control of a large number of I/O path elements in its failure recovery techniques.

12. **Referring to claim 10**, the host bus adapter of *Jantz* as modified above in claim 9, teaches that the failover actions are selected by the failover mechanism from a failover rule set [see column 2 – lines 19-33.]

13. **Referring to claim 11**, the host bus adapter of *Jantz* as modified above in claim 9, teaches that the failover mechanism is further configured to determine at the time of the detecting, operating conditions within the data storage system, to determine whether the operating conditions match a set of failover conditions, and if matching, to select the failover action corresponding to the operating conditions [see column 2 – lines 19-33; column 1 – lines 25-48, 'RDAC'.]

14. **Referring to claim 12**, the host bus adapter of *Jantz* as modified above in claim 9, teaches that the failover conditions are specific to the detected redundancy failure [see column 2 – lines 19-33; column 1 – lines 25-48, 'RDAC'; column 8 – lines 45-67; column 9 – 10-67, 'RDAC'.]

15. **Referring to claim 13**, the host bus adapter of *Jantz* as modified above in claim 9, teaches that the failover mechanism presents a single logical unit number (LUN) entity to operating system device drivers in the host processor that is discoverable a plurality of times [see column 5 – lines 42-52; column 6 – lines 26-38] and wherein the failover actions are initiated without prior communication with the host processor [see column 1 – lines 25-48, 'RDAC'.]

16. **Referring to claim 14**, *Jantz* teaches a data storage system with redundant data storage, comprising: a host computer device with a processor running operating system devices drivers

[see figure 1 – element 104; figure 3 – element 302; column 6 – lines 57-61]; a communication fabric for carrying digital data signals [see figure 1 – elements 105, 106]; an active controller controlling access by the host computer device to data storage devices [see figure 1 – element 110 ]; a standby controller controlling access by the host computer device to the data storage devices [see figure 1 – element 112 ]; and a host bus adapter linked to the host processor and the communication fabric for selecting a path through the communication fabric to one of the active and standby controllers for providing the operating system device drivers with access to the data storage devices, wherein host bus adapter is configured to initiate a failover action selected from a set of failover actions [see figure 3 – elements 302, 304, 312; column 1 – lines 25-48, 'RDAC'; column 8 – lines 45-67; column 9 – 10-67, 'RDAC'; figure 1 – elements 104, 105, 106; column 5 – lines 8-41] although, *Jantz* does not explicitly set forth the limitation of detecting failover condition with a host bus adapter. *Jantz* teaches to perform detecting failover condition with a software module called "RDAC" that may be operable within a host bus adapter [see column 1 – lines 25-48] to enable it to encompass control of a larger number of I/O path elements in its failure recovery techniques.

One of ordinary skill in the art would have clearly recognized that it was quite advantageous for the host bus adapter of the *Jantz* to detect failover condition and responding to the failover condition to encompass control of a large number of I/O path elements in its failure recovery techniques. It is for this reason that one of ordinary skill in the art would have been motivated to implement failover detecting module onto the host bus adapter in order to encompass control of a large number of I/O path elements in its failure recovery techniques.

17. **Referring to claim 15**, the data storage system of *Jantz* as modified in claim 14, teaches that the host bus adapter detects a potential failure in redundancy and determines whether to initiate the failover action by determining whether failover operating circumstances and failover operating conditions for the potential failure are satisfied [see column 2 – lines 19-33; column 1 – lines 25-48, 'RDAC'.]

18. **Referring to claim 16**, the data storage system of *Jantz* as modified in claim 14, teaches that the failover operating circumstances require when an active path in the communication fabric fails that at least one path to the controllers is available and that a path to the standby controller is usable [see column 2 – lines 19-33; column 1 – lines 25-48, 'RDAC'.]

19. **Referring to claim 17**, the data storage system of *Jantz* as modified in claim 14, teaches that the initiated failover action is selected from the set of failover actions based on existing ones of the failover operating conditions [see column 2 – lines 19-33; column 1 – lines 25-48, 'RDAC'.]

20. **Referring to claim 18**, the data storage system of *Jantz* as modified in claim 14, teaches that the data storage devices are grouped into subsets [see figure 1 – element 116; see column 5 – lines 42-52; column 6 – lines 26-38] and wherein the host bus adapter is configured to perform the failover action for the subsets when a particular storage device within the subset requires the failover action [see column 1 – lines 25-48, 'RDAC' .]

21. **Referring to claim 20**, the data storage system of *Jantz* as modified in claim 14, teaches that the host bus adapter presents a single logical unit number (LUN) entity to each of the operating system device drivers that is discoverable multiple times [see column 5 – lines 42-52; column 6 – lines 26-38.]

***Response to Arguments***

22. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents have been made record of to further show the state of the art as it pertains to systems with failover and failback firmware:

a. Tawil et al. U.S. Patent Number: 6,625,747

b. Deitz et al. U.S. Patent Number: 6,578,158

c. Beardsley et al. U.S. Patent Number : 6,061,750

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Niketa I. Patel whose telephone number is (703) 305 4893. The examiner can normally be reached on M-F 8:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A. Gaffin can be reached on (703) 308 3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NP
02/26/2004

REHANA PERVEEN
PRIMARY EXAMINER